REMARKS

A substitute Abstract is submitted which makes editorial amendments.

The drawings are proposed to be amended as follows:

(1) The description "PRIOR ART" has been added to Figs. 4 and 5.

(2) Reference character 3C attached to the block in the lower right-hand corner of Fig. 5 is deleted. Reference character 5B is correct.

(3) The term "use frequency" in block 18 in Fig. 1 on the right hand sides of pattern 1 and pattern 2 has been replaced with "use frequency counter".

The claims have been amended for editorial purposes. The amendments made are to more clearly set forth the invention and no amendment is made to add or delete subject matter in order to distinguish over the prior art.

Claims 1-4 stand rejected as being anticipated by the admitted prior art shown in Figs. 4 and 5.

The present invention provides a semiconductor test apparatus and a control method therefore, that can reduce the number of internal transfers of pattern files to a minimum. In the semiconductor test apparatus 11 of the present invention, the control unit 10 produces a pattern file use frequency table in the pattern file use frequency table memory 18. In a set of tests in which a predetermined number of semiconductors to be tested are tested, the use frequency of the pattern files is obtained, which is stored. This is set forth in claim 1. Furthermore, the control unit 10 reads out the pattern files based on the frequency of use that has been obtained, and rearranges the pattern files in the executive memory 17. This is set forth in claim 3.

The control unit 10 also deletes the pattern files in ascending order of the frequency of the use when the capacity of the memory becomes insufficient. This is set forth in claim 4. The transfer time for pattern files can thereby be greatly reduced and the throughput of the semiconductor testing can be greatly increased.

As is described in the present Specification, the conventional apparatus shown in Figs. 4 and 5 comprises an external memory, a buffer memory, a MIC memory and the SPG memory. The control apparatus searches a pattern data for testing a semiconductor and the searched data is transferred to the executive memory. Tests are carried out using the pattern data selected by the control apparatus.

The admitted conventional apparatus does not disclose the feature of the present invention as set forth in claims 1-4 of producing the pattern file use frequency table based on the number of times that the data of each pattern file is used. The conventional art also does not disclose the feature as set forth in claim 4 to delete the pattern files in the ascending order of the frequency of the use when the capacity of the memory becomes insufficient. Therefore, the present invention is neither anticipated nor suggested by the admitted prior art and claims 1-4 are patentable.

Claims 5-6 are rejected as being unpatentable over Lesmeister, U.S. 5,696,772 in view of Enoki, et al., U.S. 5,873,085.

Claims 5 and 6 are directed to a process of counting the use frequency of each of the plurality of pattern files in a set of tests and preparing a pattern file use frequency table.

Lesmeister discloses an integrated circuit tester including several processing nodes, each accessing a separate terminal of an IC to be tested. The Lesmeister tester comprises a host processing means for receiving the input data and converting the input data to a separate set of instructions for each of the nodes. Each set of instructions comprises an algorithm for generating a sequence of test vectors. Before starting the test, the Lesmeister tester produces a set of algorithms for generating test vectors and stores each algorithm in separate processing nodes. The test is organized into a succession of test cycles and during the test each node executes its stored algorithm and generates a separate test vector indicating an action to be taken by that node. The test vector includes test patterns for carrying out the semiconductor test.

However, the Lesmeister reference neither discloses nor suggests the features as set forth in claim 5 and its dependent claim 6 to rearrange the plurality of test patterns by the use frequency obtained by counting use frequency counter in the preliminary tests. Enoki is cited to show data

access management in which there is a count of the number of times that a file is accessed. Enoki discloses a virtual file management system constructed with a plurality of servers and a plurality of terminals that share file services provided by said servers. Although Enoki discloses a file management system, this is not related to a test apparatus for testing semiconductors using a plurality of test patterns. This has no relationship to the present invention of testing semiconductors in which the use of a file is related to a test of a device. The combination of Leismeister and Enoki is not supported and, even if made, does not meet the terms of claims 5 and 6.

Therefore, the present invention is neither anticipated nor suggested by the Lesmeister reference, and claims 5 and 6 are clearly patentable thereover.

Claims 7 and 8 are rejected as being unpatentable over Lesmeister in view of Enoki as applied to claim 5 and further in view of Toyonaga, et al., U.S. 5,479,657.

Claims 7 and 8 of the present invention, which depend from claim 5, set forth the feature to rearrange the order of the test patterns according to the use frequency and to delete the pattern files in the ascending order of the frequency of the use when the capacity of the memory becomes insufficient.

Toyonaga discloses a method and system for sorting count information in a computer. Frequencies of usage count information to be sorted are determined and accumulation information is prepared based on the frequency of usage information. Although Toyonaga discloses a system and method for storing count information in a computer, and the count information represents an order of priority of processing of a plurality of basic information unit, the Toyonaga reference is not related to storing the test patterns for testing semiconductor devices in the order of the frequency of use.

The addition of Enoki and Toyonaga to Lesmeister does not meet the basic structure as set forth in parent claim 5 for the reasons given above. Therefore, the novel and advantageous subject matter of dependent claims 7 and 8 are not disclosed by the combination of these references and the claims are allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Prompt and favorable action is requested.

Dated: June 29, 2004

Respectfully submitted,

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Attachments